Ultra-dense Optical I/O Interface for Silicon Photonic Interconnects

P. Liao[1], M.N. Sakib[1], J. Park[2], M. Wlodawski[2], V. I. Kopp[2], D. Neugroschl[2], and O. Liboiron-Ladouceur[1]
[1]Dept. of Electrical and Computer Eng., McGill University, 3480 University Street, Montreal, QC, Canada;
[2]Chiral Photonics, 26 Chapin Road, Unit 1104, Pine Brook, NJ 07058 USA.
peicheng.liao@mail.mcgill.ca

Abstract: An ultra-dense optical off-chip I/O interface consisting of 61 grating couplers matching the pitch of a commercial two-dimensional fiber array enables tremendous bandwidth density on the order of tens of Tb/s/mm^2 towards high throughput Silicon photonics.
OCIS codes: (200.4650) Optical interconnects; (130.3120) Integrated optics devices

1. Introduction

Silicon photonics exploiting cost-efficient CMOS fabrication processes has made remarkable progress towards dense photonic integration. A wide variety of electro-optics and optical devices has been implemented using a silicon-on-insulator (SOI) fabrication platform targeting diverse applications such as high-performance computing, optical communications, and on-chip optical interconnections [1,2]. The necessity for a greater number of optical inputs/outputs (I/Os) for off-chip communication comes with integration. The number of optical I/Os has been increased through both in-plane edge coupling and vertical out-of-plane surface coupling between optical fibers and photonic integrated waveguides [3,4]. For example, a multichannel tapered coupler can interface an array of single-mode fibers (SMFs) to an array of silicon (Si) waveguides with spot-size converters on a 20-μm pitch [3]. Despite good coupling efficiency and wide optical bandwidth, the scalability of the channel count is limited by the one-dimensional chip edge. Vertical grating couplers (VGCs) integrated with Si waveguides match the optical mode of standard SMFs through surface coupling enabling expansion of the number of channels in two dimensions. Further, high channel density (number of I/Os per area) and the layout flexibility of the chip surface contribute to more efficient utilization of the chip real estate and reduce propagation loss of routing waveguides from and to the I/Os. Currently, typical spacing between VGCs is 127 μm for standard fiber arrays, limiting the channel density at the interface of Silicon photonic integrated circuits (PICs). A pitch reducing optical fiber array (PROFA) has been developed with a reduced pitch ranging from 35 to 50 μm. A 37-channel and a 61-channel two-dimensional optical interface have been demonstrated [4,5].

In this paper, we experimentally demonstrate the feasibility of an optical I/O bandwidth density of 27 Tb/s/mm^2 using a dense Silicon photonic (SiP) interface with an hexagonal array of 61 compact VGCs on a 42.3-μm pitch, matching a two-dimensional PROFA. The scalability towards even higher channel count for increased bandwidth density and I/O throughput is discussed.

2. Ultra-dense off-chip interface design and fabrication

The silicon photonic interface is designed to match a PROFA having an hexagonal pattern of channels on 42.3 μm pitch, . The optical channels of PROFA maintain the same mode field diameter (MFD) and numerical aperture (NA) as standard SMF. Due to the small pitch, a compact VGC design [6] is used as a basic building block for the optical I/Os, as shown at the top of Fig. 1(a). Simulation based on a finite-difference time-domain (FDTD) method is performed using commercial software (Lumerical Solutions, Inc.) to optimize key parameters of the VGCs such as optical wave incident angle, grating coupler pitch, and grating duty cycle. The grating coupler length and width are optimized to meet the requirement for compact grating size, taking into account the tradeoff between compact size and increased insertion loss. The spectrum at the bottom of Fig. 1(a) is the simulation results for optical transmission of the designed grating coupler with air cladding. The transmission spectrum shows a peak centered at 1550 nm with an insertion loss of 4.0 dB for an incident angle of 20° with respect to the normal to the chip. The die surface area occupied by one PROFA interface, consisting of 61 VGCs and routing waveguides, is approximately 0.2 mm^2 (500 μm × 400 μm). The microscope image of the fabricated dense off-chip interface is shown in Fig. 1(b) with I/O channels numbered.

3. Performance assessment towards high-throughput photonic interconnection

The performance of the VGCs for the ultra-dense interface is characterized using a PROFA polished at 13° for optimum angle of incidence based on Snell's law. All 61 optical cores of the PROFA fiber are simultaneously aligned to the corresponding VGCs on the chip in a single active alignment step, as shown in Fig. 1(c). The schematic of the experimental setup is illustrated in Fig. 2(a) consisting of an optical broadband source at the input, with a polarization controller (PC) to apply transverse electric (TE) mode at the input of VGCs. A rotation stage in

the (x,y) plane is used to optimally align the chip with the polishing axis of the PROFA. Active optical alignment is achieved using directly connected VGC pairs. In Fig. 2(b), the fiber-to-fiber transmissions of nine directly connected VGC pairs are reported with a wavelength peak centered at around 1550 nm as designed. Best-case insertion loss is approximately 4.5 dB with 50 nm of bandwidth (3 dB). Compared to simulation results of 4 dB, the additional 0.5-dB loss results mainly result from imperfect alignment between the PROFA and the off-chip interface. Enhanced insertion loss performance may be realized through fabrication process optimization for the grating coupler [7]. Fixing and stabilizing the PROFA to the SiP off-chip interface with an index matching adhesive will also improve the coupling efficiency. The maximum loss difference among 18 measured VGCs is 0.7 dB with an average loss of 4.8 dB. The coupling variation is caused by misalignment as well as the PROFA channel positioning error [8].

High-speed data at 48 Gb/s (NRZ-OOK) is transmitted over four adjacent connected VGCs occupying a chip surface area of 7200 μm^2. The experimental setup (Fig. 2(c)) consists of a modulator driven with a pseudo-random bit sequence (PRBS, 2^{31}-1 bits) generated by a pulse pattern generator (PPG). The modulated signal is optically broadcast to four optical signals and propagated through four of the 61 core channels of the PROFA. At the receiver (RX), a low noise figure EDFA amplifies the signals before the photodetector (PD). The bit error rate (BER) performance is measured with an error detector (ED). The BER performance as a function of the received power for back-to-back (B2B) and the four VGC pairs are presented in Fig. 2(d). Compared to B2B transmission measurements, the power penalty is 0.5 dB at a BER of 10^{-9} and increases to 1.5 dB at a BER of 10^{-4}. There is an insignificant power penalty between the four VGC pairs demonstrating good uniformity. The aggregate bandwidth for the four channels is 192 Gb/s, corresponding to an on-chip bandwidth density of approximately 27 Tb/s/mm^2 for the designed PROFA interface. These results can be scaled to a total capacity for ultra-dense interface of 1.44 Tb/s using all 61 channels within a footprint of 0.096 mm^2. The capacity can be further increased by expanding the number of WDM channels per I/Os (VGC).

4. References

[1] B. Jalali, et al., IEEE JLT, vol. 24, no. 12, 2006.
[2] D.A.B. Miller, Proceedings of IEEE, vol. 97, no. 7, 2009.
[3] B. G. Lee, et al., OFC, PDPA4, 2010.
[4] V. I. Kopp, et al., OFC, Th5C4, 2012.
[5] P. Liao, et al., IEEE PTL, vol. pp, no. 99, 2015.
[6] F. Van Laere, et al., IEEE PTL, vol. 19, no. 23, 2007.
[7] D. Vermeulen, et al., OSA Opt. Express, vol. 18, no. 17, 2010.
[8] D. Taillaet, et al., Jpn, J. Appl. Phys., vol 45, no 8, 2006.

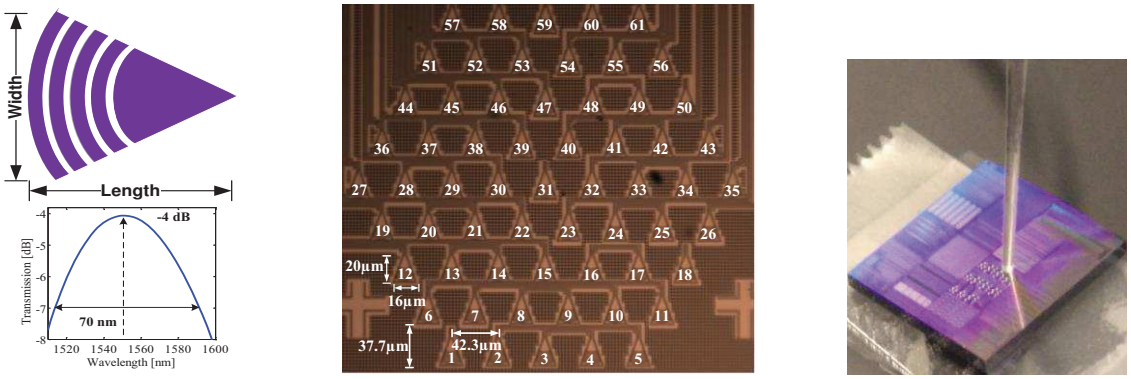

Fig. 1. (a) Vertical grating coupler (VGC) layout (top) and the simulated transmission of grating coupler (bottom) (c) Image of the two-dimensional dense SiP interface with 61 labelled VGCs with indicated horizontal and vertical pitch of 42.3 µm and 37.7 µm, respectively, (c) picture of PROFA tip aligned to SiP chip.

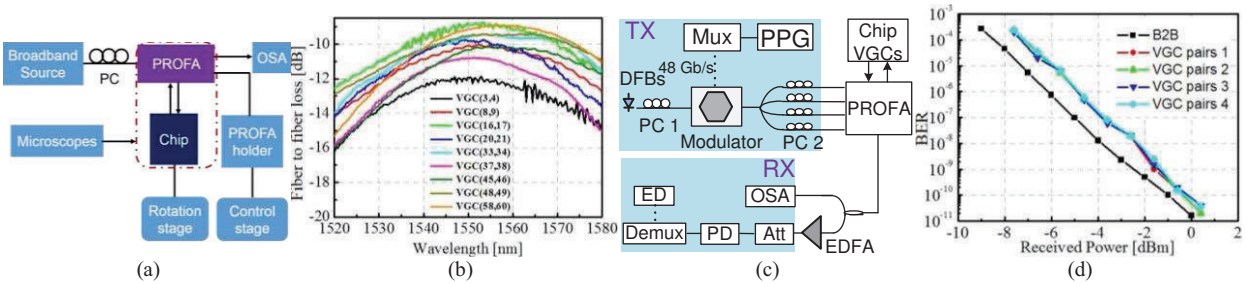

Fig. 2. (a) Schematic of experimental setup, (b) transmission spectra of designed grating couplers, (c) Experimental setup of high-speed data transmission, (d) the BER as a function of received power for back-to-back, VGC pairs data transmission.