# Co-design of an FPGA-based Low-latency Controller for MZI-based SiP Switches

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***Abstract*— A low-latency centralized controller integrated to a Silicon photonic (SiP) switch is demonstrated. The FPGA-based controller sets the configuration of a 4×4 Mach-Zehnder Interferometer-based Spanke-Beneš switch and generates traffic patterns.**

**Keywords— Optical Communications; Optical Switch; Switch Controller; Field Programmable Gate Array (FPGA)**

## I. Introduction

Since the introduction of photonic devices for high throughput communication infrastructures, most of the research focus stood on the physical layers and their improvement. Although this fact has brought important advancements on available devices (*e.g.*, as in [1]), this leads to a gap between system-level designs and physical-level designs. While physical designers keep working on components improvement, system level designers focus on higher-level aspects, such as the system control [2]. For feasibility demonstration, it remains crucial to further pursue and investigate integrating advances of both fields [3]. Here, we present a complete setup where both system and physical layers are co-designed towards an efficient demonstration of photonic integration potential.

## II. Centralized SiP Switch Controller

Fig. 1 presents an overview of the switch system setup consisting of both network and physical layers. The interface of the two layers is done using available ports of the FPGA, such as General Purpose I/O (GPIO) and SMA ports. For the proposed setup, a 10 MHz operation frequency is used due to bandwidth limitation of GPIO ports. Also, only input ports 1 and 2 and output port 2 of the switch were used to ease the initial data visualization.

The system layer is entirely deployed using Altera's FPGAs technology executing the following tasks: 1) the system controller, namely our novel Look-up Table Centralized Controller (LUCC) algorithm [2], 2) data pattern generators, 3) fast transceivers units serializing and de-serializing the payload data, and 4) an error detector unit allocating temporary memories to store the generated payload and the received payload data for error detection purpose. The LUCC controller is based on a look-up table with a modified iSLIP algorithm [4] for low-latency configuration of the SiP switch. The multistage MZI-based switch consists of five MZIs that are configured in bar (ON) or crossbar (OFF) state based on input port request and contention resolution results [2]. The SiP chip was fabricated through the IME foundry and exhibits switching time of approximately 6 ns. Details of the SiP switch performance can be found in [1]. The 4×4 MZI-based Spanke-Beneš switch is integrated with signal converters, used between the electrical domain of the interconnect ports (*e.g.*, processor, memory), and the optical domain of the SiP switch (not shown in this setup). The generated payload traffic is modulated and injected into input ports of the switch (port 1 and 2 in this setup). After proper data routing, a photodetector collects payload data at the output ports (output port 2 in this setup) of the switch.

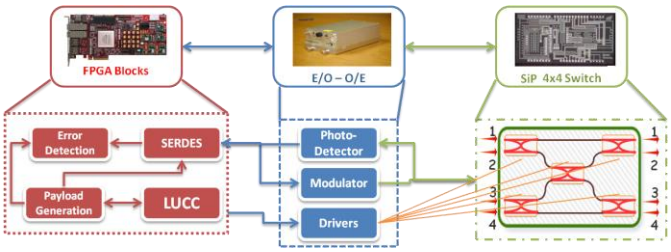


Fig.1: Controlled SiP switch system setup overview.

Beyond scheduling, the FPGA-based system executes payload traffic of various patterns (*e.g.*, PRBS, alternating bits) for initial physical layer testing. The traffic patterns are configurable. To verify for possible errors in the system, the error detection unit compares the received payload data against the generated data. If an error is found, the erroneous data is stored for further investigation. If no problem is found, the payload data is discarded for the following packets. This way, this work presents one step forward on the advances of SiP technology integration on system-level design.

## III. References

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